LISTING OF CLAIMS

1. (Original) A computer-implemented method for creating an electronic circuit design, comprising:

providing a plurality of user-selectable system-level design objects, each system-level design object defined by a system-level function;

providing a plurality of hardware-level design objects, each hardware-level design object configured to generate a hardware definition of a hardware-level function, wherein one or more hardware-level design objects are combinable to implement each system-level design object;

instantiating a system-level design in a system-level design file, the system-level design including user-selected ones of the system-level design objects; and

simulating behavior of the system-level design consistent with the system-level functions and behavior of a hardware definition from the hardware-level design objects that implement the user-selected ones of the system-level design objects.

2. (Original) The method of claim 1, wherein each system-level design object is parameterizable and has associated therewith at least one input data port or at least one output data port, and each input and output data port has an associated, user-specified sample rate, the method further comprising:

in response to a signal to generate a hardware-level design from the system-level design file,

supplementing the system-level design objects with clock-clear and clock-enable ports;

generating a clock control hardware definition that includes output ports for each different sample rate, with each clock-enable port coupled to a clock control output port having a rate corresponding to the associated sample rate;

identifying for each system-level design object one or more hardware-level design objects that implement the system-level design object; and

generating hardware definitions using hardware definition generators that are associated with the hardware-level design objects.

3. (Original) The method of claim 2, further comprising:

simulating behavior of the system-level design with user-specified input-data generators that generate system-level input data;

capturing the system-level input data generated by the input-data generators; and

generating a hardware definition for a first testbench component that provides the system-level input data as input data to the hardware definitions.

4. (Original) The method of claim 3, further comprising simulating behavior of the design defined by the hardware definitions and the testbench component.

5. (Original) The method of claim 4, further comprising:

capturing system-level output data generated during simulation of the system-level design;

generating a hardware definition for a second testbench component that compares output data generated during simulation of the design defined by the hardware definitions to output data captured during simulation of the system-level design.

6. (Original) The method of claim 1, further comprising:

simulating behavior of the design defined in the system-level design file with user-specified input-data generators that generate system-level input data;

capturing the system-level input data generated by the input-data generators; and

generating a hardware definition for a first testbench component that provides the system-level input data as input data to the hardware definitions.

7. (Original) The method of claim 6, further comprising simulating behavior of the design defined by the hardware definitions and the testbench component.

8. (Original) The method of claim 7, further comprising:

capturing system-level output data generated during simulation of the design defined in the system-level design file;

generating a hardware definition for a second testbench component that compares output data generated during simulation of the design defined by the hardware definitions to output data captured during simulation of the design defined in the system-level design file.

9. (Original) An apparatus for creating an electronic circuit design, comprising:

means for providing a plurality of user-selectable system-level design objects, each system-level design object defined by a system-level function;

means for providing a plurality of hardware-level design objects, each hardware-level design object configured to generate a hardware definition of a hardware-level function, wherein one or more hardware-level design objects are combinable to implement each system-level design;

means for instantiating a system-level design in a system-level design file, the system-level design including user-selected ones of the system-level design objects; and

means for simulating behavior of the system-level design consistent with the system-level functions and behavior of a hardware definition from the hardware-level design objects that implement the user-selected ones of the system-level design objects.

10. (Original) The apparatus of claim 9, wherein each system-level design object is parameterizable and has associated therewith at least one input data port or at least one output data port, and each input and output data port having an associated, user-specified sample rate, further comprising:

responsive to a signal to generate a hardware-level design from the system-level design file,

means for supplementing the system-level design objects with clock-enable

and clock-clear ports;

means for generating a clock control hardware definition that includes output ports for each different sample rate, with each clock-enable port coupled to a clock control output port having a rate corresponding to the associated sample rate;

means for identifying for each system-level design object one or more hardware-level design objects that implement the system-level design object; and

means for generating hardware definitions using hardware definition generators that are associated with the hardware-level design objects.

11. (Previously Presented) A system for creating an electronic circuit design, comprising:

a plurality of user-selectable system-level design objects, each system-level design object defined by a system-level function;

a plurality of hardware-level design objects, each hardware-level design object configured to generate a hardware definition of a hardware-level function, wherein one or more hardware-level design objects are combinable to implement each system-level design;

a computing arrangement that hosts a system-level simulator, wherein the simulator is configured to instantiate a system-level design in a system-level design file, the system-level design including user-selected ones of the system-level design objects, and simulate behavior of the system-level design consistent with the system-level functions and behavior of a hardware definition from the hardware-level design objects that implement the user-selected ones of the system-level design objects.

12. (Original) The system of claim 11, wherein each system-level design object is parameterizable and has associated therewith at least one input data port or at least one output data port, and each input and output data port having an associated, user-specified sample rate, further comprising a translator coupled to the system-level simulation environment, the translator configured to, responsive to a signal to generate a hardware-level design from the system-level design file,

supplement the system-level design objects with clock-enable and clock-clear

ports;

generate a clock control hardware definition that includes output ports for each different sample rate, with each clock-enable port coupled to a clock control output port having a rate corresponding to the associated sample rate;

identify for each system-level design object one or more hardware-level design objects that implement the system-level design object; and

generate hardware definitions using hardware definition generators that are associated with the hardware-level design objects.

13. (Original) The system of claim 12, wherein the system-level simulation environment is configured to:

simulate behavior of the system-level design with user-specified input-data generators that generate system-level input data;

capture the system-level input data generated by the input-data generators; and

generate a hardware definition for a first testbench component that provides the system-level input data as input data to the hardware definitions.

14. (Original) The system of claim 13, wherein the system-level simulation environment is configured to:

capture system-level output data generated during simulation of the system-level design; and

generate a hardware definition for a second testbench component that compares output data generated during simulation of the design defined by the hardware definitions to output data captured during simulation of the system-level design.